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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,214	03/29/2002	Timothy S. Lehner	BUR920010175US1	7092

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/063,214	LEHNER ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-8 and 10 (all pending claims) were rejected in the office action of 16 October 2006. Applicants' response submitted on 16 January 2007 has cancelled claims 1-8 and 10 and presented new claims 37-51.

The status of the claims in Applicants' remarks and the listing of the claims submitted on 16 January 2007 are presumed to be in error. The current status of the claims is believed to be:

Claims 1-36 are cancelled; and

Claims 37-51 are new.

If this understanding is in error, clarification is respectfully requested.

Claims 37-51 are pending in this application. Claims 37-51 are rejected.

Prior Art

1. The following portion of Applicants' remarks submitted on 16 January 2007 are regarded as admitted prior art.

> Applicants submit that "iSsPICE4 User's Guide" by Intusoft does not anticipate Applicants' now claimed invention. Most notably, IsSpice4 is a circuit simulator which can be used to perform an overall circuit simulation on a design which includes Applicants' claimed encapsulated circuit model (See Intusoft pg. 13 last paragraph, and Lehner p37 and 38). Additionally, IsSpice4 could be *used* by the proprietary circuit designer to calculate the parameter values (Ip, In, Cm, Cin, Cout) stored in memory (Lehner Fig. 6 box 63) using the method steps described in Applicants' specification paragraphs 37-43. The collective parameters stored in memory make up the encapsulated circuit model and this is what is given to the customer. A Spice simulator is simply a tool for practicing Applicants' invention, including building and/or simulating the novel circuit model (Lehner Fig. 2-5). In fact, IsSpice4 is a simulator which can be used as the "circuit simulator program" defined in Applicants' claims 37 and 45. However, Intosoft's IsSpice4 simulator is not "...an encapsulated circuit model stored in the memory which is behaviorally equivalent to an original circuit... the encapsulated circuit model stored in the memory exhibits none of a plurality of circuit details from the original circuit." (pages 16-17, emphasis in original)

Specification

2. The amendments to the specification submitted on 16 October 2006 were not entered for reasons set forth in the previous office action. In response, Applicants' submit that:

> Applicants have amended paragraphs: 31, 38, 46, 79, and 95 to comply with requests for correction outlined in the Office Action pages 4-5. Applicants further submit that a single bracket ("[ ]") indicates wording that is not represented in a quotation, but exists in the actual documentation from which the quote is taken. Double brackets ("[[ ]]"), however, is the proper representation for a deletion edit. Therefore, Applicants contend that the amendments to the specification in the 7/6/06 response are correctly represented.

37 CFR 1.121 makes no provision for indicating "wording that is not represented in a quotation, but exists in the actual documentation from which the quote is taken." 37 CFR 1.121 specifically states in relevant part that:

> Amendments to the specification, other than the claims, computer listings (§ 1.96) and sequence listings (§ 1.825), must be made by adding, deleting or replacing a paragraph, by replacing a section, or by a substitute specification, in the manner specified in this section.

Where Applicants' representative has previously submitted a **replacement paragraph**, 37 CFR 1.121 specifically states in relevant part that:

> The full text of any replacement paragraph with markings to show all the changes relative to the previous version of the paragraph. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strikethrough cannot be easily perceived

Applicants' attention is respectfully drawn to the requirement to provide **the full text of any replacement paragraph**. There is no provision in 37 CFR 1.121 for the use of single brackets as described in Applicants' current response.

The amendments to specification submitted on 16 January 2007 will be entered as presented. It is unclear if Applicants' remarks constitute a request to enter the amendments to the specification submitted on 6 July 2006.

The 6 July 2006 amendments alter the text of paragraphs 62 and 87. These amendments, if entered, will delete the following subject matter from the specification:

Paragraph 62: "of the model element values, at all values of all I/O node voltages. This step is necessary since the invention assumes all element values depend on all I/O node voltages. The input node voltages are also explicitly functions of time, as given by the input voltage waveforms."

Paragraph 87: "The inputs to this function are the detailed waveforms (class SIM_Wave, for example) at the circuit inputs and a load description (either a simple capacitance, a pi- model, another static load model, or a call-back function) at the circuit outputs. The load model is not restricted to a pi model or a simple capacitance. As in the ideal current source model method described in the first embodiment, the model could be any other static load model, or a dynamic call-back function." Also, "The call-back function allows the user or calling program to choose the optimum load, a very useful feature for embedding these models in a multi-vendor methodology, where the circuit model and the load model may come from different vendors. The invention provides the prototype(s) of the call-back(s) function. Also, the invention could potentially have more than one call-back interface (prototype)."

In responding to this office action, the Examiner respectfully requests that Applicants provide clear instruction regarding the 6 July 2006 amendments to the specification. They will be entered upon Applicants' request because, as previously noted, they are technically in compliance with 37 CFR 1.121. If so requested, paragraphs 62 and 87 will be changed in accordance with those amendments, deleting the subject matter indicated above. This deletion may cause difficulties under 35 U.S.C. § 11g2, first paragraph.

The previous objections to the specification have been withdrawn.

Claim Objections

3. Claims 37 and 45 are objected to because of the following informalities: The claims recite verbose limitations that appear to obfuscate what Applicants are seeking to patent.

Independent claim 37 recites "the output node value is a function of the first and second current value, the first input voltage value, the first output voltage value, and the first, second and third capacitance value; wherein the first and second current value, and the first, second, and third capacitance value, is calculated by the computer system as a function of the first input voltage value and the first output voltage value." Independent claim 45 recites similar language.

This lengthy recitation of functional dependency merely defines that "the output node value is calculated by the computer system as a function of the first input voltage value and the first output voltage value" because every other parameter recited by the claim language is ultimately a function of the same first input and first output voltage values.

If Applicants allege that, in the field of computer simulation of electrical circuits, "computing an output node value as a function of an input voltage and an output voltage" is novel or non-obviousness, clarification of that point is respectfully requested.

4. Claims 37 and 45 are objected to because of the following informalities: These claims contain a period within the body of the claim. Appropriate correction is required.

5. Claim 49 is objected to because of the following informalities: The phrase "each having an output voltage value each having an output voltage value" appears to be a typographical error.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The previous rejections of claims 1-8 and 10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement are withdrawn. These claims have been cancelled.

The previous rejections of claims 1-8 and 10 under 35 U.S.C. § 112, second paragraph, as being indefinite are withdrawn. These claims have been cancelled.

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 37-51 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Independent claims 37 and 45 recite "an encapsulated circuit model ...: being behaviorally equivalent to an original circuit," wherein "the encapsulated circuit model ... exhibits none of a plurality of circuit details from the original circuit."

The requirement that the circuit model be simultaneously "behaviorally equivalent" and "exhibit none of a plurality of circuit details of the original circuit" appears to lie beyond the subject matter supported by the specification because of the conflicting nature of these limitations. A person of ordinary skill in the art would understand a circuit model that is "behaviorally equivalent" to an original circuit to exhibit at least one circuit detail of the original circuit, specifically its behavior.

7. Claims 42 and 49 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Although the scope of claims 42 and 49 are indefinite (see below), the claimed subject matter, specifically the plural pluralities of first and second current sources, does not appear to find support under 35 U.S.C. § 112, first paragraph, in the application as filed. Clarification of the claimed subject matter may overcome this rejection.

Claim 49 is rejected for similar rationale.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 37-51 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claim 37 is indefinite for the following reasons.

Claim 37 recites that "the encapsulated circuit model ... exhibits none of a plurality of circuit details from the original circuit" which plainly conflicts with the first limitation which recites "an encapsulated circuit model ... being behaviorally equivalent to an original circuit."

Claim 37 recites that "the encapsulated circuit model ... exhibits none of a plurality of circuit details from the original circuit" and in no way limits the breadth of the phrase "a plurality of circuit details from the original circuit." It is noted that the claim requires that the circuit model comprises, *inter alia*, "at least one output node and one input node." The claim appears to define via implication that the recited "original circuit" does not have "at least one output node and one input node." Similar grounds of rejection apply to the other recited components of the circuit model.

Claim 45 is rejected for similar rationale.

9. Claims 37-44 are indefinite for their various descriptions of the invention. Claims 38-44 refer to "the encapsulated circuit model of claim 37," or "the circuit model of claim 37." Claim

42, in independent form, refers to both. Claim 37 defines "a memory for access by a circuit simulation program." It is unclear whether Applicants regard "a memory," "an encapsulated circuit model," or simply "a circuit model" as the invention.

10. Claims 45-51 are indefinite for their various descriptions of the invention. Claims 46-51 refer to "the encapsulated circuit model of claim 45," or "the circuit model of claim 45." Claim 37 defines "a memory for access by a circuit simulation program." It is unclear whether Applicants regard "a memory," "an encapsulated circuit model," or simply "a circuit model" as the invention.

11. Claim 42 is indefinite for the following reasons.

Claim 42 recites "a plurality of the input nodes" and "for each of the input nodes ... is a plurality of the first current sources." It is unclear if this means that the claimed invention comprises plural pluralities of first current sources. It is unclear where support for this interpretation is found in the drawings or specification, however this appears to be the literal meaning of the claim language. Similar rationale is applied to the "plurality of second current sources".

The phrase "the input nodes" lacks antecedent basis.

The phrase "the first current sources" lacks antecedent basis.

The phrase "the second capacitors" lacks antecedent basis.

12. Claim 49 is indefinite for the following reasons.

Claim 49 recites "a plurality of the input nodes" and "for each of the input nodes ... is a plurality of the first current sources." It is unclear if this means that the claimed invention comprises plural pluralities of first current sources. It is unclear where support for this interpretation is found in the drawings or specification, however this appears to be the literal meaning of the claim language. Similar rationale is applied to the "plurality of second current sources".

The phrase "the first current sources" lacks antecedent basis.

The phrase "the input nodes" lacks antecedent basis.

The phrase "the second capacitors" lacks antecedent basis.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Claim Rejections - 35 USC § 102

The previous rejections under 35 U.S.C. § 102 are withdrawn because the pending claims have been cancelled. Applicants' arguments have been fully considered and are found persuasive to the extent that they are quoted above in the section labeled "Prior Art".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

13. Claims 35-51 are rejected under 35 U.S.C. § 103(a) as being unpatentable over "IsSpice4 User's Guide" by Intusoft in view of "Star-Hspice Manual" by Avant! Corporation.

According to Applicants' remarks submitted on 16 January 2007, "IsSpice4 is a simulator which can be used as the "circuit simulator program" defined in Applicants' claims 37 and 45."

IsSpice4 does not expressly teach the "encapsulated circuit model" defined by claims 37 and 45.

Star-Hspice teaches the "encapsulated circuit model" defined by claims 37 and 45. See Figure 20-10. For Applicants' convenience, the Examiner has included a blown-up copy of Figure 20-10 with markings to correspond with FIG. 5 of the instant application.

Star-Hspice and IsSpice4 are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art to combine the teachings of Star-Hspice and IsSpice4 by using the "AC noise equivalent circuit" taught by Star-Hspice (FIG. 20-10) in a circuit simulation as taught by IsSpice4 in order to perform a noise and AC analysis of a MOSFET (Star-Hspice, page 9, last paragraph).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Star-Hspice and IsSpice4 in order to arrive at the invention specified in claims 37 and 45.

Conclusion

14. Claims 37-51 are rejected under 35 U.S.C. § 112, first and second paragraphs. Detailed rejections of these claims under 35 U.S.C. §§ 102 and 103 would be improper for relying upon speculative interpretation according to MPEP 2143.03, which states:

> A claim limitation which is considered indefinite cannot be disregarded. If a claim is subject to more than one interpretation, at least one of which would render the claim unpatentable over the prior art, the examiner should reject the claim as indefinite under 35 U.S.C. 112, second paragraph (see MPEP § 706.03(d)) and should reject the claim over the prior art based on the interpretation of the claim that renders the prior art applicable. *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984) (Claims on appeal were rejected on indefiniteness grounds only; the rejection was reversed and the case remanded to the examiner for consideration of pertinent prior art.). Compare *In re Wilson*, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious) and *In re Steele*, 305 F.2d 859,134 USPQ 292 (CCPA 1962) (it is improper to rely on speculative assumptions regarding the meaning of a claim and then base a rejection under 35 U.S.C. 103 on these assumptions).

The prior art has applied to the Examiner's best understanding of what Applicants seek to patent based upon the text of the claims and the disclosure of the application.

Although claims 38-44 and 46-51 are not specifically rejected under 35 U.S.C. §§ 102 or 103, this fact should not be interpreted as an indication of allowable subject matter.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

3/9/07

DETAILED ACTION

Claims 1-8 and 10 (all pending claims) were rejected in the office action of 16 October 2006. Applicants' response submitted on 16 January 2007 has cancelled claims 1-8 and 10 and presented new claims 37-51.

The status of the claims in Applicants' remarks and the listing of the claims submitted on 16 January 2007 are presumed to be in error. The current status of the claims is believed to be:

Claims 1-10 are cancelled;

Claims 11-22 are withdrawn via the office action of 6 April 2006;

Claims 23-36 are withdrawn via the office action of 16 October 2006; and

Claims 37-51 are new.

If this understanding is in error, clarification is respectfully requested.

Claims 37-51 are pending in this application. Claims 37-51 are rejected.

Prior Art

1. The following portion of Applicants' remarks submitted on 16 January 2007 are regarded as admitted prior art.

> Applicants submit that "iSsPICE4 User's Guide" by Intusoft does not anticipate Applicants' now claimed invention. Most notably, IsSpice4 is a circuit simulator which can be used to perform an overall circuit simulation on a design which includes Applicants' claimed encapsulated circuit model (See Intusoft pg. 13 last paragraph, and Lehner p37 and 38). Additionally, IsSpice4 could be *used* by the proprietary circuit designer to calculate the parameter values (Ip, In, Cm, Cin, Cout) stored in memory (Lehner Fig. 6 box 63) using the method steps described in Applicants' specification paragraphs 37-43. The collective parameters stored in memory make up the encapsulated circuit model and this is what is given to the customer. A Spice simulator is simply a tool for practicing Applicants' invention, including building and/or simulating the novel circuit model (Lehner Fig. 2-5). In fact, IsSpice4 is a simulator which can be used as the "circuit simulator program" defined in Applicants' claims 37 and 45. However, Intosoft's IsSpice4 simulator is not

> "...an encapsulated circuit model stored in the memory which is behaviorally equivalent to an original circuit... the encapsulated circuit model stored in the memory exhibits none of a plurality of circuit details from the original circuit." (pages 16-17, emphasis in original)

Specification

2. The amendments to the specification submitted on 16 October 2006 were not entered for reasons set forth in the previous office action. In response, Applicants' submit that:

> Applicants have amended paragraphs: 31, 38, 46, 79, and 95 to comply with requests for correction outlined in the Office Action pages 4-5. Applicants further submit that a single bracket ("[ ]") indicates wording that is not represented in a quotation, but exists in the actual documentation from which the quote is taken. Double brackets ("[[ ]]"), however, is the proper representation for a deletion edit. Therefore, Applicants contend that the amendments to the specification in the 7/6/06 response are correctly represented.

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> Amendments to the specification, other than the claims, computer listings (§ 1.96) and sequence listings (§ 1.825), must be made by adding, deleting or replacing a paragraph, by replacing a section, or by a substitute specification, in the manner specified in this section.

Where Applicants' representative has previously submitted a **replacement paragraph**, 37 CFR 1.121 specifically states in relevant part that:

> The full text of any replacement paragraph with markings to show all the changes relative to the previous version of the paragraph. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strikethrough cannot be easily perceived

Applicants' attention is respectfully drawn to the requirement to provide **the full text of any replacement paragraph**. There is no provision in 37 CFR 1.121 for the use of single brackets as described in Applicants' current response.

The amendments to specification submitted on 16 January 2007 will be entered as presented. It is unclear if Applicants' remarks constitute a request to enter the amendments to the specification submitted on 6 July 2006.

The 6 July 2006 amendments alter the text of paragraphs 62 and 87. These amendments, if entered, will delete the following subject matter from the specification:

Paragraph 62: "of the model element values, at all values of all I/O node voltages. This step is necessary since the invention assumes all element values depend on all I/O node voltages. The input node voltages are also explicitly functions of time, as given by the input voltage waveforms."

Paragraph 87: "The inputs to this function are the detailed waveforms (class SIM_Wave, for example) at the circuit inputs and a load description (either a simple capacitance, a pi- model, another static load model, or a call-back function) at the circuit outputs. The load model is not restricted to a pi model or a simple capacitance. As in the ideal current source model method described in the first embodiment, the model could be any other static load model, or a dynamic call-back function." Also, "The call-back function allows the user or calling program to choose the optimum load, a very useful feature for embedding these models in a multi-vendor methodology, where the circuit model and the load model may come from different vendors. The invention provides the prototype(s) of the call-back(s) function. Also, the invention could potentially have more than one call-back interface (prototype)."

In responding to this office action, the Examiner respectfully requests that Applicants provide clear instruction regarding the 6 July 2006 amendments to the specification. They will be entered upon Applicants' request because, as previously noted, they are technically in

compliance with 37 CFR 1.121. If so requested, paragraphs 62 and 87 will be changed in accordance with those amendments, deleting the subject matter indicated above. This deletion may cause difficulties under 35 U.S.C. § 11g2, first paragraph.

The previous objections to the specification have been withdrawn.

Claim Objections

3. Claims 37 and 45 are objected to because of the following informalities: The claims recite verbose limitations that appear to obfuscate what Applicants are seeking to patent.

Independent claim 37 recites "the output node value is a function of the first and second current value, the first input voltage value, the first output voltage value, and the first, second and third capacitance value; wherein the first and second current value, and the first, second, and third capacitance value, is calculated by the computer system as a function of the first input voltage value and the first output voltage value." Independent claim 45 recites similar language.

This lengthy recitation of functional dependency merely defines that "the output node value is calculated by the computer system as a function of the first input voltage value and the first output voltage value" because every other parameter recited by the claim language is ultimately a function of the same first input and first output voltage values.

If Applicants allege that, in the field of computer simulation of electrical circuits, "computing an output node value as a function of an input voltage and an output voltage" is novel or non-obviousness, clarification of that point is respectfully requested.

4. Claims 37 and 45 are objected to because of the following informalities: These claims contain a period within the body of the claim. Appropriate correction is required.

5. Claim 49 is objected to because of the following informalities: The phrase "each having an output voltage value each having an output voltage value" appears to be a typographical error.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The previous rejections of claims 1-8 and 10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement are withdrawn. These claims have been cancelled.

The previous rejections of claims 1-8 and 10 under 35 U.S.C. § 112, second paragraph, as being indefinite are withdrawn. These claims have been cancelled.

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 37-51 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described

in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Independent claims 37 and 45 recite "an encapsulated circuit model ... being behaviorally equivalent to an original circuit," wherein "the encapsulated circuit model ... exhibits none of a plurality of circuit details from the original circuit."

The requirement that the circuit model be simultaneously "behaviorally equivalent" and "exhibit none of a plurality of circuit details of the original circuit" appears to lie beyond the subject matter supported by the specification because of the conflicting nature of these limitations. A person of ordinary skill in the art would understand a circuit model that is "behaviorally equivalent" to an original circuit to exhibit at least one circuit detail of the original circuit, specifically its behavior.

7. Claims 42 and 49 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Although the scope of claims 42 and 49 are indefinite (see below), the claimed subject matter, specifically the plural pluralities of first and second current sources, does not appear to find support under 35 U.S.C. § 112, first paragraph, in the application as filed. Clarification of the claimed subject matter may overcome this rejection.

Claim 49 is rejected for similar rationale.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 37-51 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claim 37 is indefinite for the following reasons.

Claim 37 recites that "the encapsulated circuit model ... exhibits none of a plurality of circuit details from the original circuit" which plainly conflicts with the first limitation which recites "an encapsulated circuit model ... being behaviorally equivalent to an original circuit."

Claim 37 recites that "the encapsulated circuit model ... exhibits none of a plurality of circuit details from the original circuit" and in no way limits the breadth of the phrase "a plurality of circuit details from the original circuit." It is noted that the claim requires that the circuit model comprises, *inter alia*, "at least one output node and one input node." The claim appears to define via implication that the recited "original circuit" does not have "at least one output node and one input node." Similar grounds of rejection apply to the other recited components of the circuit model.

Claim 45 is rejected for similar rationale.

9. Claims 37-44 are indefinite for their various descriptions of the invention. Claims 38-44 refer to "the encapsulated circuit model of claim 37," or "the circuit model of claim 37." Claim 42, in independent form, refers to both. Claim 37 defines "a memory for access by a circuit simulation program." It is unclear whether Applicants regard "a memory," "an encapsulated circuit model," or simply "a circuit model" as the invention.

10. Claims 45-51 are indefinite for their various descriptions of the invention. Claims 46-51 refer to "the encapsulated circuit model of claim 45," or "the circuit model of claim 45." Claim 37 defines "a memory for access by a circuit simulation program." It is unclear whether Applicants regard "a memory," "an encapsulated circuit model," or simply "a circuit model" as the invention.

11. Claim 42 is indefinite for the following reasons.

Claim 42 recites "a plurality of the input nodes" and "for each of the input nodes ... is a plurality of the first current sources." It is unclear if this means that the claimed invention comprises plural pluralities of first current sources. It is unclear where support for this interpretation is found in the drawings or specification, however this appears to be the literal meaning of the claim language. Similar rationale is applied to the "plurality of second current sources".

The phrase "the input nodes" lacks antecedent basis.

The phrase "the first current sources" lacks antecedent basis.

The phrase "the second capacitors" lacks antecedent basis.

12. Claim 49 is indefinite for the following reasons.

Claim 49 recites "a plurality of the input nodes" and "for each of the input nodes ... is a plurality of the first current sources." It is unclear if this means that the claimed invention comprises plural pluralities of first current sources. It is unclear where support for this interpretation is found in the drawings or specification, however this appears to be the literal meaning of the claim language. Similar rationale is applied to the "plurality of second current sources".

The phrase "the first current sources" lacks antecedent basis.

The phrase "the input nodes" lacks antecedent basis.

The phrase "the second capacitors" lacks antecedent basis.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Claim Rejections - 35 USC § 102

The previous rejections under 35 U.S.C. § 102 are withdrawn because the pending claims have been cancelled. Applicants' arguments have been fully considered and are found persuasive to the extent that they are quoted above in the section labeled "Prior Art".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

13. Claims 35-51 are rejected under 35 U.S.C. § 103(a) as being unpatentable over "IsSpice4 User's Guide" by Intusoft in view of "Star-Hspice Manual" by Avant! Corporation.

According to Applicants' remarks submitted on 16 January 2007, "IsSpice4 is a simulator which can be used as the "circuit simulator program" defined in Applicants' claims 37 and 45."

IsSpice4 does not expressly teach the "encapsulated circuit model" defined by claims 37 and 45.

Star-Hspice teaches the "encapsulated circuit model" defined by claims 37 and 45. See Figure 20-10. For Applicants' convenience, the Examiner has included a blown-up copy of Figure 20-10 with markings to correspond with FIG. 5 of the instant application.

Star-Hspice and IsSpice4 are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art to combine the teachings of Star-Hspice and IsSpice4 by using the "AC noise equivalent circuit" taught by Star-Hspice (FIG. 20-10) in a circuit simulation as taught by IsSpice4 in order to perform a noise and AC analysis of a MOSFET (Star-Hspice, page 9, last paragraph).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Star-Hspice and IsSpice4 in order to arrive at the invention specified in claims 37 and 45.

Conclusion

14. Claims 37-51 are rejected under 35 U.S.C. § 112, first and second paragraphs. Detailed rejections of these claims under 35 U.S.C. §§ 102 and 103 would be improper for relying upon speculative interpretation according to MPEP 2143.03, which states:

> A claim limitation which is considered indefinite cannot be disregarded. If a claim is subject to more than one interpretation, at least one of which would render the claim unpatentable over the prior art, the examiner should reject the claim as indefinite under 35 U.S.C. 112, second paragraph (see MPEP § 706.03(d)) and should reject the claim over the prior art based on the interpretation of the claim that renders the prior art applicable. *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984) (Claims on appeal were rejected on indefiniteness grounds only; the rejection was reversed and the case remanded to the examiner for consideration of pertinent prior art.). Compare *In re Wilson*, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious) and *In re Steele*, 305 F.2d 859,134 USPQ 292 (CCPA 1962) (it is improper to rely

on speculative assumptions regarding the meaning of a claim and then base a rejection under 35 U.S.C. 103 on these assumptions).

The prior art has applied to the Examiner's best understanding of what Applicants seek to patent based upon the text of the claims and the disclosure of the application.

Although claims 38-44 and 46-51 are not specifically rejected under 35 U.S.C. §§ 102 or 103, this fact should not be interpreted as an indication of allowable subject matter.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
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3/8/07

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